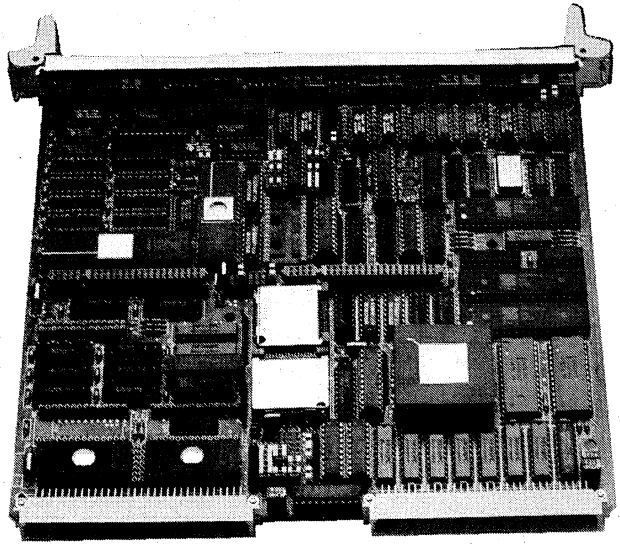
iSBC® 186/410 MULTIBUS® II SERIAL COMMUNICATIONS COMPUTER

- **Six Serial Communication Channels on a Single MULTIBUS® II Board, Expandable to 10 Channels via iSBX™ Bus Connectors**
- **High Integration 8 MHz 80186 Microprocessor**
- **82258 Advanced DMA Controller Provides 4 Independent High Performance DMA Channels**
- **Supports RS232C-Only on 4 Channels, RS422A or RS232C Interface Configurable on 2 Channels**
- **512K Bytes DRAM Provided**
- **MULTIBUS® II iPSB (Parallel System Bus) Interface with Full Message Passing Capability**
- **Four 28-Pin JEDEC Sites, Expandable to 8 Sites with iSBC® 341 MULTIMODULE™ for a Maximum of 512K Bytes EPROM**
- **Two iSBX™ Connectors for Low Cost I/O Expansion**
- **MULTIBUS® II Interconnect Space for Software Configurability and Diagnostics**
- **Resident Firmware to Support Host-to-Controller Download Capability and Built-In-Self-Test (BIST) Diagnostics**

The iSBC 186/410 MULTIBUS II Serial Communications Computer is an intelligent 6-channel communications processor implementing the full, high performance message passing interface of the MULTIBUS II (iPSB) Parallel System Bus. This iSBC board combines an 8 MHz 80186 16-bit microprocessor, with six serial channels (expandable to 10 serial channels on-board via iSBX connectors), up to 512K bytes of DRAM, four 28-pin JEDEC sites, two iSBX connectors, and an 82258 ADMA controller on a single 220 mm x 233 mm (8.7 in. x 9.2 in.) Eurocard printed circuit board. The iSBC 186/410 board supports asynchronous, byte synchronous, and bit-synchronous (HDLC/SDLC) communications protocols on the two full/half duplex RS232C/RS422A channels, and asynchronous-only on the four full/half duplex RS232C-only channels. Acting as a terminal controller or front-end processor, this board adds significant data communications flexibility to an OEM's MULTIBUS II design.



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Order Number: 280268-002

OPERATING ENVIRONMENT

The iSBC 186/410 MULTIBUS II Serial Communications Computer is a powerful data communications sub-system specifically designed to operate in and support the message-based, multi-processor system configurations being implemented on the MULTIBUS II architecture. The board's on-board CPU, an 8 MHz 80186 microprocessor, provides significant intelligence to off-load and distribute the serial communications functions away from one or all of a system's processor boards.

The iSBC 186/410 board was designed with a set of features to address several communications application areas: terminal/cluster controller, or front-end processor.

Terminal/Cluster Controller

A terminal/cluster controller concentrates communications in a central area of a system. Efficient handling of messages coming in or going out of the system requires sufficient buffer space to store messages along with high speed I/O channels to transmit and receive those messages. Sophisticated cluster controller applications also require character and format conversion capabilities to allow attachment of different types of terminals.

The iSBC 186/410 MULTIBUS II Serial Communications Computer is well suited for multi-terminal system applications (see Figure 1). Up to 10 serial channels can be serviced in multi-user or cluster configurations by adding two iSBX 354 Dual Serial Channel MULTIMODULE boards. The on-board 512K byte (expandable to 512K bytes) DRAM array is the buffer area designed to handle incoming and outgoing messages at data rates up to 19.2K baud (asynch). Each serial channel can be individually programmed for different baud rates to allow system configurations with differing terminal types. The on-board 80186 CPU handles the protocols and character manipulation tasks traditionally performed by a system host.

Front-end Processor

A front-end processor off-loads a system's central processor of bandwidth-draining tasks such as data manipulation and text editing of characters collected from the attached serial I/O devices. Since most ter-

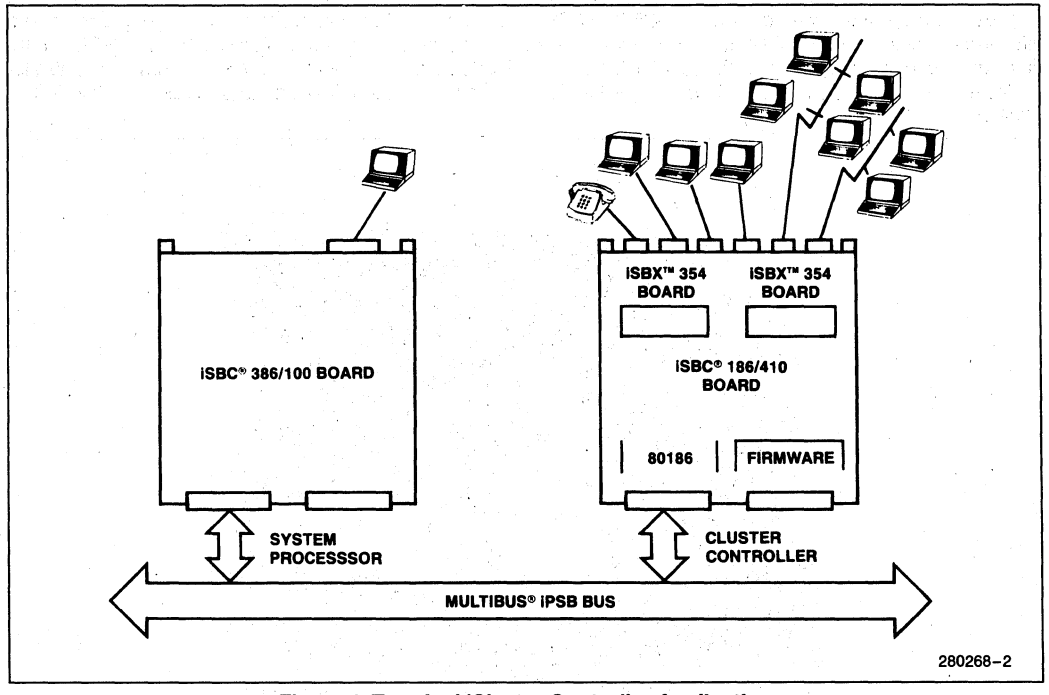

Figure 1. Terminal/Cluster Controller Application

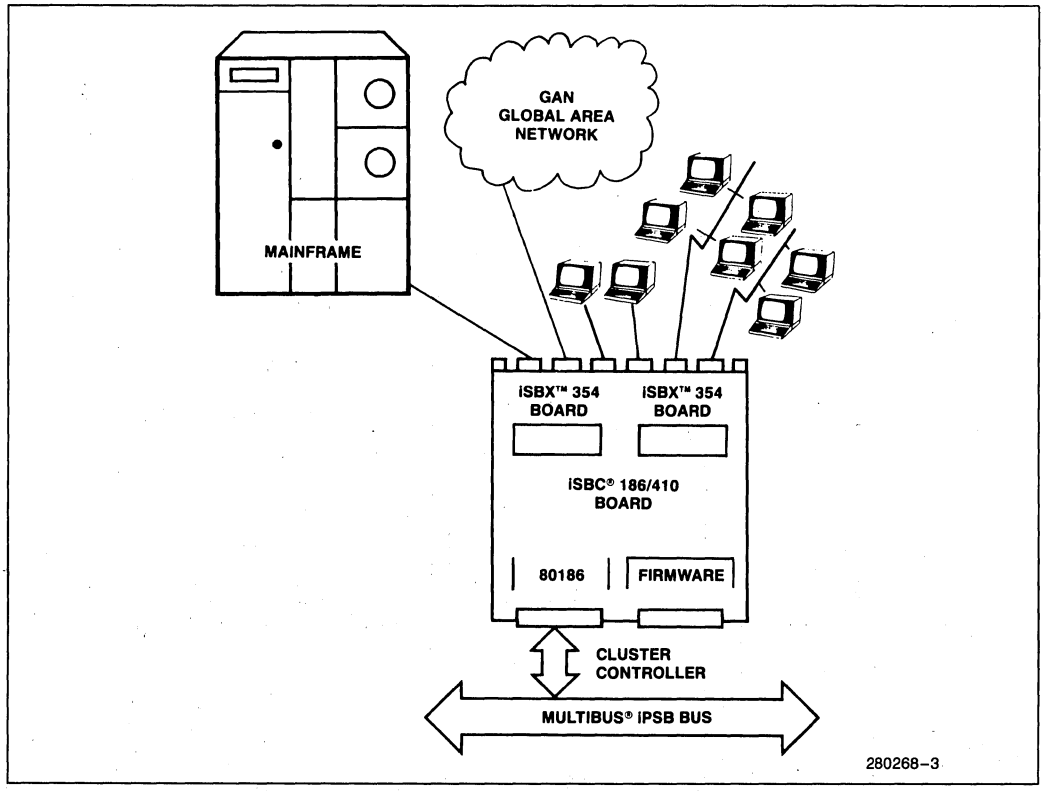

Figure 2. Front-End Processor Application

minal and serial I/O devices require flexible interfaces, program code is often dynamically downloaded to the front-end processor from a system CPU. Downloading code requires sufficient memory space for protocol handling and program code. Flow control and interrupt handling requirements need an efficient real time operating software environment to manage the hardware and software resources on the board.

The iSBC 186/410 board features are designed to provide a high performance solution for front-end processor applications (see Figure 2). A large amount of memory is provided for dynamic storage of program code. Two serial channels (as well as four iSBX expansion serial channels) can be configured for links to mainframe systems, point-to-point terminals, modems or multi-drop designs and four serial channels are for terminal communication, asynchronous RS232C operation only.

ARCHITECTURE

The iSBC 186/410 MULTIBUS II Serial Communications Computer consists of six major subsystem areas: Processor, Serial I/O, Memory, General I/O, iPSB bus interface, and Interconnect (see Figure 3).

Processor Subsystem

80186 PROCESSOR

The central processor unit on the iSBC 186/410 board is Intel's 16-bit 8 MHz 80186 microprocessor. The highly integrated 80186 CPU combines several system components onto a single chip (i.e., two Direct Memory Access lines, three Interval Timers, Clock Generator, and Programmable Interrupt Controller). The 80186 instruction set is a superset of the 8086 and maintains object code compatibility while adding additional instructions.

This high performance component manages the board's multi-user, multi-protocol communications operations. Refer to the Microsystem Components Handbook, Order Number 230843-00X, for more detailed information on the hardware operation and requirements of the 80186 microprocessor component.

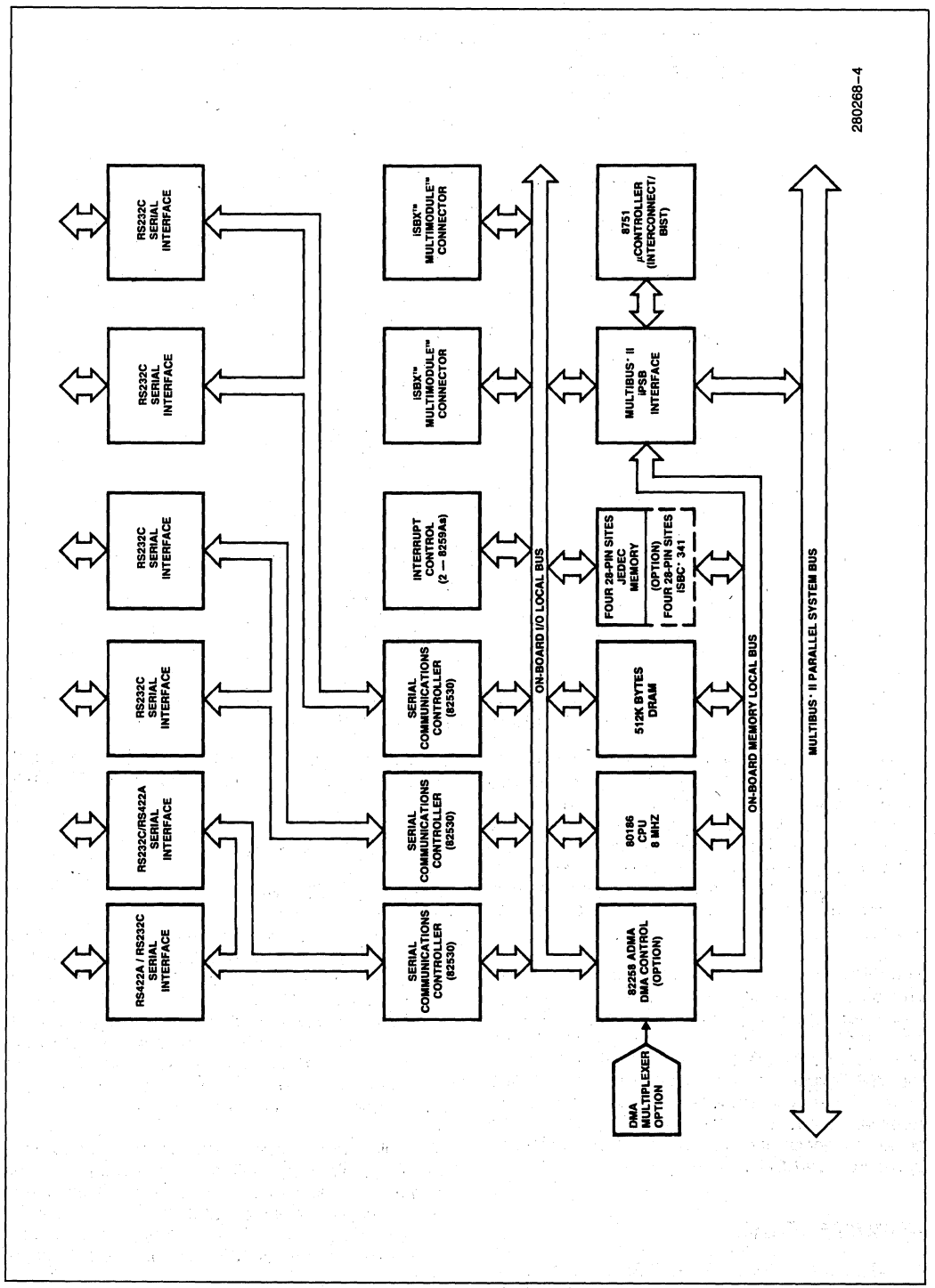

Figure 3. iSBC® 186/410 Board Functional Block Diagram

DIRECT MEMORY ACCESS (DMA) FUNCTION

The iSBC 186/410 board provides 13 channels of DMA to support serial I/O, iPSB interface, and/or iSBX bus transfer operations. The 80186 microprocessor provides two DMA channels, the 82258 Advanced (ADMA) controller supports three "direct" channels of DMA, and the ADMA multiplexer circuit uses the fourth 82258 ADMA channel providing eight additional multiplexed DMA channels. The allocation of the board's DMA channels to on-board resources is listed in Table 1.

SERIAL I/O SUBSYSTEM

Six serial interfaces are provided on the iSBC 186/410 board: two interfaces support full asynchronous, byte-synchronous, and bit-synchronous (HDLC/SDLC) communication and four interfaces support asynchronous-only communication. The two RS422A configurable ports can also be tri-stated to allow multi-drop networks. The board's serial capability can be expanded to 10 channels by adding two iSBX 354 Dual Channel Serial I/O MULTIMODULE boards. Each added iSBX 354 board uses an

Table 1. iSBC® 186/410 Board DMA Channel Allocation

Channel Count		Channel Number	DMA Configuration Local Bus Resource
80186			
1	DMA Channel	0	Half-Duplex High Speed Serial Interface (SCC1 Channel A) (—High Density 15-Pin Connector)
2	DMA Channel	1	Full-Duplex Serial Interface (SCC1 Channel A) or SBX1 DMA Request
82258 ADMA			
3	DMA Channel	0	Input DMA from MPC (Message Passing Coprocessor)
4	DMA Channel	1	Output DMA to MPC
5	DMA Channel	2	Half-Duplex High Speed Serial Interface (SCC1 Channel B) (—High Density 15-Pin Connector) or SBX1 DMA REQ
	DMA Channel	3	Full-Duplex High Speed Serial Interface (SCC1 Channel B) or INT2 DMA REQ from DMA Multiplexer
DMA Multiplexer*			
6	DMA Channel	0	Half-Duplex Serial Interface (SCC2 Chan. A, 9-pin conn.)
7	DMA Channel	1	Full-Duplex Serial Interface (SCC2 Chan. A)
8	DMA Channel	2	Half-Duplex Serial Interface (SCC2 Chan. B, 9-pin conn.)
9	DMA Channel	3	Full-Duplex Serial Interface (SCC2 Chan. B) or SBX1 DMA Request or Half-Duplex SCC1 Channel B.
10	DMA Channel	4	Half-Duplex Serial Interface (SCC3 Chan. A, 9-pin conn.)
11	DMA Channel	5	Full-Duplex Serial Interface (SCC3 Chan. A) or SBX2 DMA Request
12	DMA Channel	6	Half-Duplex Serial Interface (SCC3 Chan. B, 9-pin conn.)
13	DMA Channel	7	Full-Duplex Serial Interface (SCC3 Chan. B) or INT1 SBX1 for SBX344

NOTE:
*ADMA Channel 3 is used to add the DMA Multiplexer.

82530 SCC component to provide two independent full duplex serial channels configurable as either RS232C or RS422A interfaces. It also supports both asynchronous or programmable byte and bit synchronous (HDLC/SDLC) protocols. The HDLC/SDLC interface is compatible with IBM system and terminal equipment and with CCITT's X.25 packet switching interface.

Three 82530 Serial Communications Controllers (SCCs) provide six channels of half/full serial I/O. Two channels are configurable as either RS232C or RS422 on two high density 15-pin female D-shell connectors. Four more channels are RS232C-only using IBM standard 9-pin male D-shell connectors. All six channels directly support the Data Terminal Equipment (DTE) configuration, with the Data Communication Equipment (DCE) pin-out supported by changes in the cable wiring.

The 82530 component is designed to satisfy several serial communications requirements; asynchronous, byte-synchronous, and bit-synchronous (HDLC/SDLC) modes. The increased capability at the serial controller point results in off-loading a CPU of tasks normally assigned to the CPU or its associated hardware. Configurability of the 82530 allows the user to configure it to handle all asynchronous data formats regardless of data size, number of start or stop bits, or parity requirements. An on-chip baud rate generator allows independent baud rates on each channel.

Memory Subsystem

The iSBC 186/410 board's on-board memory subsystem consists of a large DRAM array and a set of universal memory sites. Access to the on-board memory subsystem resources, as well as off-board iPSB bus access, is accomplished by observing the iSBC 186/410 board memory map (see Figure 4). The mapping occurs within the 1 megabyte memory space of the 80186 microprocessor, and is split into three main areas: DRAM reserved, iPSB window, and EPROM reserved. The first 0 to 512K bytes is always reserved for local DRAM, the next 128K or

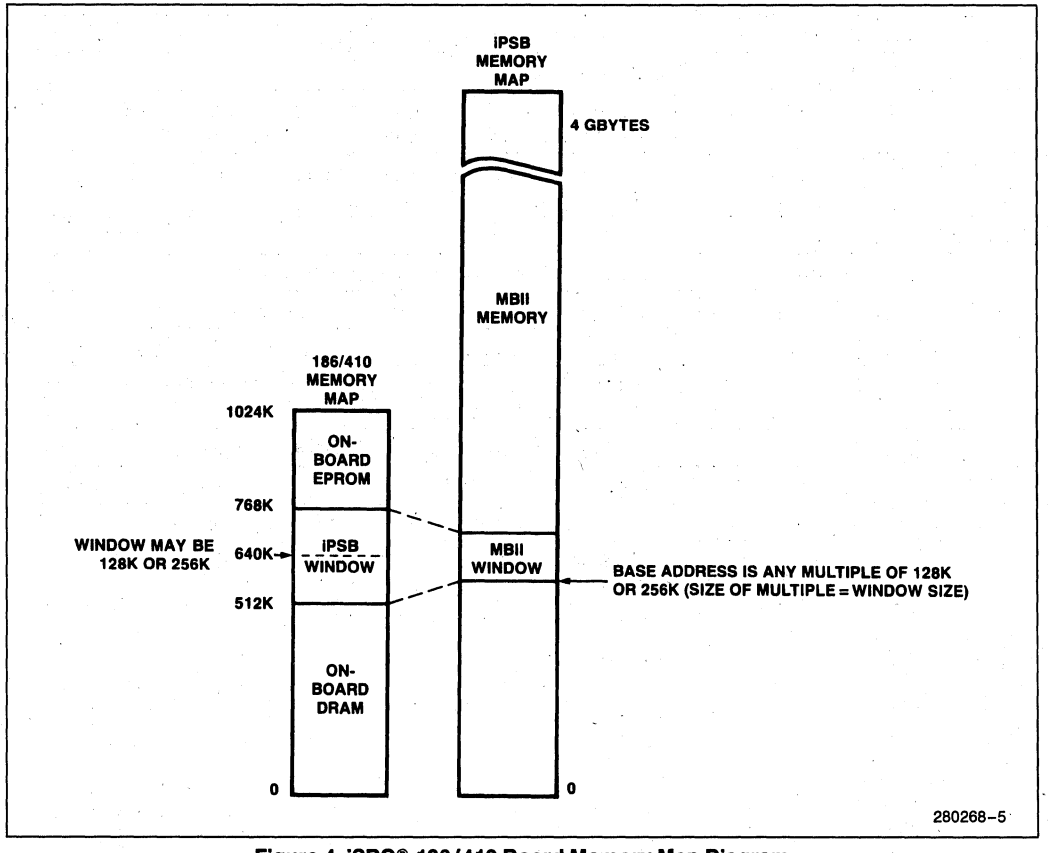

Figure 4. iSBC® 186/410 Board Memory Map Diagram

256K bytes (or up to 768K) is the iSPB window, and the remaining 384K or 256K byte area is reserved for local EPROM. The iPSB window maps a 128K or 256K byte local memory area into the 4 gigabyte global physical address range of the MULTIBUS II iPSB bus. This window is programmable and allows the 80186 processor to access the complete 4 gigabyte memory space of the iPSB bus.

The board's memory map also supports a 64K byte access window for I/O space between local and iPSB bus access. The 64K bytes of local I/O space is mapped 1-to-1 to the iPSB bus' 64K byte I/O space and is not programmable. The upper 32K bytes access the iPSB bus I/O space, and the lower 32K bytes are reserved for local on-board I/O.

DRAM CAPABILITIES

The iSBC 186/410 board comes standard with a 512K byte DRAM memory array on-board.

EPROM MEMORY

A total of four 28-pin JEDEC universal sites reside on the iSBC 186/410 board. These sockets support addition of byte-wide ROM and EPROM devices in densities from 8K bytes (2764) to 64K bytes (27512) per device. Two of the four sockets contain a pair of 27812 EPROM devices installed at the factory(1). These devices contain 128K bytes of firmware providing both the Host-to-controller download routine and the Built-In-Self-Test (BIST) power-up diagnostics routine. The remaining two sockets allow the user to add either two additional devices or an iSBC 341 EPROM MULTIMODULE for a maximum of 512K bytes.

NOTE:
(1) These devices may be removed by the user for access to the two 28-pin sites.

General I/O Subsystem

The I/O subsystem provides timers, interrupt control and two IEEE P959 iSBX connectors for I/O expansion or customization.

PROGRAMMABLE TIMERS AND INTERRUPT CONTROL

The 80186 microprocessor on the iSBC 186/410 board provides three independent, fully programmable 16-bit interval timers/event counters for use by the systems designer to generate accurate time intervals under software control. The outputs may be independently routed to a PIC to count external events. The system software configures each timer independently and can read the contents of each counter at any time during system operation.

In a MULTIBUS II system, external interrupts (interrupts originating from off-board) are interrupt type messages over the iPSB bus rather than signals on individual lines. Interrupt type messages are handled by the bus interface logic, the MPC Message Passing Coprocessor chip. The MPC component interrupts the 80186 processor via an 8259A Programmable Interrupt Controller (PIC) indicating a message has been received. This means that 1 Interrupt line can handle interrupts from up to 255 sources.

Two on-board 8259A PICs are used in a master-slave configuration for processing on-board interrupts. One of the interrupt lines handles the interrupt messages received from the iPSB bus. Table 2 includes a list of devices and functions supported.

iSBX™ BUS I/O EXPANSION

Two 8/16-bit iSBX bus (IEEE P959) connectors are provided for modular, low-cost I/O expansion. The iSBC 186/410 board supports both 8-bit and 16-bit iSBX MULTIMODULEs through these mating, gas-tight pins and socket connectors. DMA is also supported to the iSBX connectors and can be configured by programming the DMA multiplexor attached to the 82258 ADMA component. The iSBX connectors on the iSBC 186/410 board support a wide variety of standard iSBX compatible boards from Intel and other independent vendors providing add-on functions such as, floppy control, ¼" tape control, bubble memory, parallel/serial I/O, BITBUS™ interface, math, graphics, IEEE 488, and analog I/O. Custom iSBX module designs are also supported as per the IEEE P959 iSBX bus specification.

iPSB Bus Interface Subsystem

This subsystem's main component is the Message Passing Coprocessor chip. Subsystem services provided by the MPC bus interface component include full message passing support and memory, I/O, and interconnect access to the iPSB bus by the 80186 processor. The single-chip Message Passing Coprocessor is a highly integrated CHMOS device implementing the full message passing protocol and performing all the arbitration, transfer, and exception cycle protocols specified in the MULTIBUS II Architecture Specification Rev. C., Order Number 146077.

Table 2. iSBC® 186/410 Board Interrupt Devices and Functions

Device	Function	Number of Interrupts
iPSB Bus Interface (MPC)	Message-Based Interrupt Requests from the iPSB bus via MPC Message Passing Coprocessor	1 interrupt for up to 255 sources
8751 Interconnect Controller	Interconnect Space	1
80186 Timers & Interrupt	Timers 0 and 1 and Interrupt Acknowledge 1	3
82530 SCCs (3 devices)	SCC #1 and SCC #2 or SCC #3 for Transmit Buffer Empty, Receive Buffer Full, and Channel Errors	2
iPSB Bus Interface (MPC)	Indicates Transmission Error on iPSB Bus	1
82258 ADMA	DMA Transfer Complete	1
IEEE P959 iSBX Bus Connectors (2)	Functions Determined by iSBX Bus MULTIMODULE Boards	4 (2/connector)
IEEE P959 iSBX Bus Connectors (2)	DMA Interrupt from iSBX (TDMA)	2

Interconnect Subsystem

MULTIBUS II interconnect space is a standardized set of software configurable registers designed to hold and control board configuration information as well as system and board level diagnostics and testing information. Interconnect space is implemented with the 8751 microcontroller and the MPC silicon resident on the iSBC 186/410 board.

The read-only registers store information such as board type, vendor I.D., firmware rev. level, etc. The software configurable registers are used for auto-software configurability and remote/local diagnostics and testing.

Firmware Capability

HOST/CONTROLLER SOFTWARE DOWNLOAD ROUTINE

Resident in ROM on this controller is a host-to-controller software download routine to support the downloading of communication firmware into the iSBC 186/410 Serial Communication Computer. This loader adheres to the MULTIBUS II Download Protocol and responds to commands issued by software running on a host CPU board. The host CPU passes these commands to the loader via registers defined in the board's interconnect space. A download function, a commence execution function, and an examine local memory function are all provided in the routine. Data transfers are supported by both shared memory systems and message based systems. The top 1K of DRAM on the board is reserved for the exclusive use of the download program. Host CPUs must not overwrite this area with download commands.

Software on the host is responsible for accessing the iSBC 186/410 board's firmware on disk or from ROM visible to the host and translating it into linear sequences of bytes suitable for downloading (see Figure 5). After downloading the firmware, the host issues a command for the loader routine on the controller to begin execution of the downloaded software.

BUILT-IN SELF-TEST DIAGNOSTICS

On-board built-in self-test (BIST) diagnostics provide a customer confidence test of the various functional areas on the iSBC 186/410 board. The initialization checks are performed by the 8751 microcontroller, while the BIST package is executed by the 80186 microprocessor. On-board tests included in the BIST package are: DRAM, EPROM, 80186, 82530 SCCs, and the MPC.

Additional activities performed include initialization at power-up using the Initialization and Diagnostics Executive and a program table check, a feature allowing users to add custom code in EPROM while still maintaining full use of factory supplied BISTs. Immediately after power-up and initialization of the 8751 microcontroller, the 80186 microprocessor begins its own initialization and on-board diagnostics. Upon successful completion of these activities, the Initialization and Diagnostics Executive invokes the user-defined program table. A check is made of the program table which then executes user-defined custom programs.

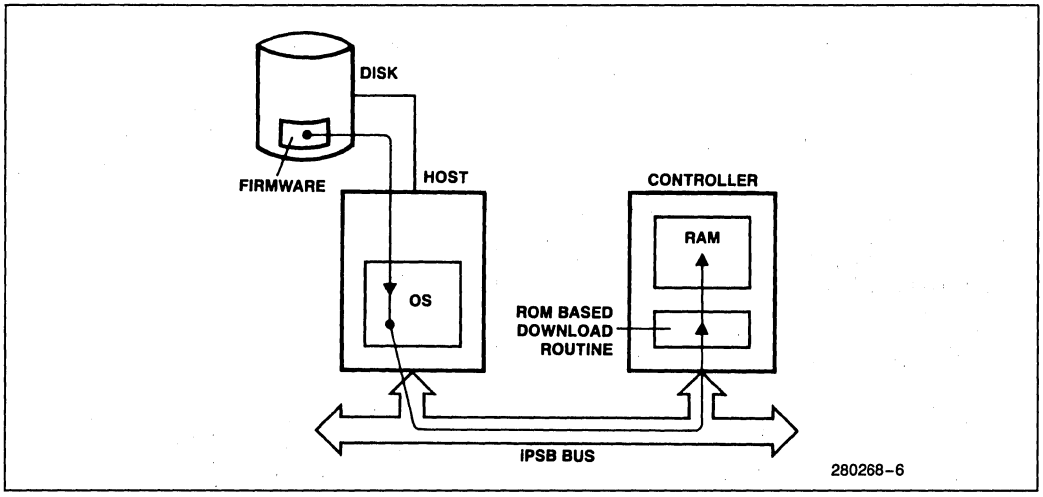

Figure 5. Download Routine

The BIST package provides a valuable testing, error reporting and recovery capability on MULTIBUS II boards enabling the OEM to reduce manufacturing and maintenance costs. An LED on the board's front panel indicates the status of power-up diagnostics. It is on when BIST diagnostics start running and is turned off upon successful completion of the BISTs.

SPECIFICATIONS

Word Size

Instruction: 8-, 16-, 24-, 32-, 40-, or 48-bits

Data: 8- or 16-bits

System Clock

CPU: 8.0 MHz

Cycle Time

Basic Instruction: 8.0 MHz—500 ns

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., 4 clock cycles).

Memory Capacity

Local Memory

DRAM—512K bytes on-board (64K x 4-bit devices); 8 sockets provided to support additional 256K bytes

EPROM—Number of sockets—four 28-pin JEDEC sites

EPROM	Device Size (Bytes)	Max. Memory Capacity
2764	8K	32K bytes
27128	16K	64K bytes
27256	32K	128K bytes
27512	64K	256K bytes

NOTE:
**EPROM Expansion to up to a maximum of 512K bytes is achieved via attachment of the iSBC 341 EPROM (256K byte) MULTIMODULE board.

I/O Capability

Serial—Six programmable serial channels using three 82530 Serial Communications Controller components.

I/O Expansion—Two 8/16-bit IEEE P959 iSBX connectors (DMA supported). (The board supports either two single wide or one double-wide form factor iSBX module(s).)

Timers—Three programmable timers on the 80186 microprocessor.

Input Frequencies—Frequencies supplied by the internal 80186 16 MHz crystal; 82530 SCCs: crystal driven at 9.8304 MHz div. by two; iSBX Connector: crystal driven at 9.8304 MHz.

Serial Communications Characteristics

Synchronous—Internal or external character synchronization on one or two synchronous characters.

Asynchronous—5—8 data bits and 1, 1½ or 2 stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.

Baud Rates

Synchronous X1 Clock (Channels 0, 1)	
Baud Rate	**82530 Count Value (Decimal)**
64000	36
48000	49
19200	126
9600	254
4800	510
2400	1022
1800	1363
1200	2046
300	8190
Asynchronous X16 Clock (Channels 0–5)	
Baud Rate	**82530 Count Value (Decimal)**
19200	6
9600	14
4800	30
2400	62
1800	83
1200	126
300	510
110	1394

Serial Signals/Pin-Outs

RS232C Interface Pin Assignment for High Density 15-Pin Connectors

J2 Pin	RS-232C Pin Number	RS-232C Signal Name	RS-232C Signal Function
1	1	TXD	Transmit Data
2	2	RTS	Request To Send
3	3	RXD	Receive Data
4	4	CTS	Clear To Send
5	5	RXC	Receive Clock
6	6	DSS	Data Signal Select
7	7	DTR	Data Terminal Ready
8	8	DSR	Data Set Ready
9	9	DCD	Carrier Detect
10	10	STXC	Transmit Clock
11	11	SGD	Signal Ground
12	12	LCLPBK	Local Loopback
13	13	RMLPBK	Remote Loopback
14	14	TSTMD	Test Mode Indicator
15	15	RNG	Not Supported

RS422A Interface Pin Assignment for High Density 15-Pin Connectors

J1 Pin	Signal Name On Board	RS-422A Signal Name	RS-422A Signal Function
1	RS42211	TR (a)	Transmit Data
2		(a)	Control
3	RS4229	RD (a)	Receive Data
4		(a)	Indication
5		(a)	Signal Timing
6	RS42212	TR (b)	Transmit Data
7		(b)	Control
8	RS42290	RD (b)	Receive Data
9		(b)	Indication
10		(b)	Signal Timing
11			Signal Ground
12			Not Used
13			Not Used
14			Not Used
15			Chassis Ground

NOTE:
The iSBC® 186/40 board does not support the unused signals.

RS232C Interface Pin Assignment for IBM® Compatible 9-Pin Connectors

Pin Number	Signal Name	Function	In/Out
1	CD	Carrier Detect	In
2	RXD	Received Data	In
3	TXD	Transmit Data	Out
4	DTR	Data Terminal Ready	Out
5	SG	Signal Ground	
6	DSR	Data Set Ready	In
7	RTS	Request To Send	Out
8	CTS	Clear To Send	In
9	RI	Ring Indicator	Not Supported

Interrupt Capability

Potential Interrupt Sources from iPSB Bus—255 individual and 1 Broadcast

Interrupt Levels—12 vectored requests using two 8259As and 1 input to the master PIC from the slave PIC

Interrupt Requests—All levels TTL compatible

Interfaces

iPSB Bus—Compliance Level RQA/RPA D16M32

iSBX Bus—Compliance Level D8/16 DMA

Serial I/O—2 ch. RS232C or RS422A compatible, configured DTE only; 4 ch. RS232C IBM compatible only, configured DTE only.

Connectors

Interface	Connector	Part #
iPSB bus (P1)	96-pin DIN, right angle female	603-2-IEC-C096-F
RS232C/ RS422A	15-pin high density, D type, right angle female (see note)	
RS232C-only	9-pin IBM compatible, D type, right angle male (see note)	

NOTE:
The manufacturers below provide connectors which will mate with the connectors supplied on the iSBC 186/410 board front-panel.

Mating Connectors, Shells and Cables

Connectors and Shells	Manufacturer	Pins	Part No.
High Density D-type Plug (male)	AMP	15	204501-1
High Density D-type Plug (male)	Positronic	15	DD-15M
D-type Receptacle (female)	AMP	9	205203-3
D-type Receptacle (female)	ITT-Cannon	9	DE-9S
Connector Shells	AMP	(For 15 or	745171-X
	ITT-Cannon	9-pin connect.	DE-51218
	3M	above).	358-2100
Cable Description	**Manufacturer**		**Part No.**
15 Conductor—Shield, Round	Alpha		5120/15
15 Conductor—Shield, Round	Beldon		9541
10 Conductor—Shield, Round	Alpha		5120/10
9 Conductor—Shield, Round	Beldon		9539

NOTE:
All cable referenced is available in 100 ft. minimum lengths.

PHYSICAL DIMENSIONS

The iSBC 186/410 board meets all MULTIBUS II mechanical specifications as presented in the MULTIBUS II Architecture Specification Handbook (#146077, Rev. C)

Eurocard Form Factor

Depth: 220 mm (8.7 inches)

Height: 233 mm (9.2 inches)

Front Panel Width: 20 mm (0.76 inches)

Weight: 822 gm (29 ounces)

ENVIRONMENTAL CHARACTERISTICS

Temperature

Inlet air at 200 LFM airflow over all boards
Non-operating: −40°C to +75°C
Operating: 0° to +55°C

Humidity

Non-operating—95% Relative Humidity @ +55°C, non-condensing

Operating—90% Relative Humidity @ +55°C, non-condensing

ELECTRICAL CHARACTERISTICS

The maximum power required per voltage is shown below.

Voltage (volts)	Max. Current (amps)	Max. Power (watts)
+5V	8.22A	43.16W
+12V	150 mA	1.89W
−12V	150 mA	1.89W

REFERENCE MANUALS

iSBC 186/410 Serial Communications Computer User's Guide (#148941-001)

Intel MULTIBUS II Architecture Specification Handbook (#146077)

Manuals may be ordered from any Intel Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 186/410	MULTIBUS II Serial Communications Computer